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Signed Andrew Gersey

Dated 19 August 2003

Pate. Form 1/77

Patents Act 1977
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The Patent Office

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13DEC02 E770707-1 D01063
P01/7700 0.00-0229048.4

Request for grant of a patent

(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

The Patent Office

Cardiff Road
Newport
South Wales
NP9 1RH

1. Your reference — JSR.P52288GB

2. Patent application number *(The Patent Office will fill in this part)* — 0229048.4

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

Zarlink Semiconductor Limited
Cheney Manor
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Patents ADP number *(if you know it)*

If the applicant is a corporate body, give the country/state of its incorporation — British

S2429680001

4. Title of the invention — Apparatus for and Method of Regenerating a Clock and Network Interface

5. Name of your agent *(if you have one)* — Marks & Clerk

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

4220 Nash Court
Oxford Business Park South
Oxford OX4 2RU
United Kingdom

7271125001

Patents ADP number *(if you know it)*

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing *(day / month / year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*

a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.
See note (d))

Yes

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	
Description	10
Claim(s)	3
Abstract	1
Drawing(s)	2 + 2

10. If you are also filing any of the following, state how many against each item.

Priority documents	
Translations of priority documents	
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	1
Request for preliminary examination and search *(Patents Form 9/77)*	1
Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application.

Signature [signature] Date 11 December 2002

Marks & Clerk

12. Name and daytime telephone number of person to contact in the United Kingdom: John S. Robinson - 01865 397900

Warning

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Notes

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b) *Write your answers in capital letters using black ink or you may type them.*

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Patents Form 7/77

Patents Act 1977
(Rule 15)

Statement of inventorship and of right to grant of a patent

The Patent Office

Cardiff Road
Newport
South Wales
NP9 1RH

1. Your reference — JSR.P52288GB

2. Patent application number *(if you know it)* — 0229048.4

3. Full name of the or of each applicant — Zarlink Semiconductor Limited

4. Title of the invention — Apparatus for and Method of Regenerating a Clock and Network Interface

5. State how the applicant *(s)* derived the right from the inventor *(s)* to be granted a patent — By virtue of employment.

6. How many, if any, additional Patents Forms 7/77 are attached to this form? *(see note (c))* — None

7. I/We believe that the person *(s)* named over the page *(and on any extra copies of this form)* is/are the inventor *(s)* of the invention which the above patent application relates to.

Signature
Marks & Clerk

Date
11 December 2002

8. Name and daytime telephone number of person to contact in the United Kingdom — John S. Robinson - 01865 397900

Notes

a) *If you need help to fill in this form or you have any questions, please contact the Patent Office on 0645 500505.*

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c) *If there are more than three inventors, please write the names and addresses of the other inventors on the back of another Patents Form 7/77 and attach it to this form.*

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Enter the full names, addresses and postcodes of the inventors in the boxes and underline the surnames

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Patents ADP number *(if you know it)*:

Patents ADP number *(if you know it)*:

Reminder

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APPARATUS FOR AND METHOD OF REGENERATING A CLOCK AND NETWORK INTERFACE

The present invention relates to an apparatus for and a method of regenerating a clock. The present invention also relates to a network interface comprising such an apparatus.

Adaptive clock recovery is a known concept and is disclosed, for example, in the relevant standards on circuit emulation services over ATM, ITU standard 1.363.1 and ATM Forum standard af-vtoa-0078. However, the concept is described in general terms and no implementations are disclosed.

According to a first aspect of the invention, there is provided an apparatus for regenerating a clock, comprising a buffer for buffering data packets, a counter arranged to be incremented upon arrival of each data packet by a first amount representing the amount of data in the packet and to be decremented by a second amount representing the amount of data transmitted from the apparatus, a digital filter for performing a filter function having a low pass component on the count in the counter, a digitally controlled oscillator for supplying the regenerated clock to control the timing of data transmission, and a controller for controlling the frequency of the oscillator in accordance with the filtered count.

References to "incrementing" as used herein include both incrementing in a positive direction and incrementing in a negative direction. References to "decrementing" mean changing in a direction opposite to incrementing.

The controller may be arranged to control the frequency of the oscillator so as to reduce the difference between the amount of packet data in the buffer and a predetermined amount.

The filter and the controller may be embodied as separate hardware. The filter may be embodied as hard-wired hardware.

The filter may comprise a first order low pass filter. The filter may be arranged to form a series of samples Y_n, each of which is given by:

$$Y_n = Y_{n-1} + (X_n - Y_{n-1}) / 2^P$$

where n is the sample number, X_n is the count, and P is a parameter. P may be programmable. The controller may be arranged to form a series of samples F_m representing the frequency of the oscillator and given by:

$$F_m = F_{m-1} + G1\ (Y_m - Y_{m-1}) + G2\ (Y_m - Offset)$$

Where m is the sample number and G1 and G2 are parameters. At least one of G1 and G2 may be programmable.

The counter may be arranged to be incremented by 1 upon arrival of each data packet and to be decremented by 1 upon transmission of an amount of data equal to the content of a data packet. As an alternative, the counter may be arranged to be incremented by the number of bytes in a data packet upon arrival of each data packet and to be decremented by Z upon transmission of each group of Z data bytes, where Z is a positive integer. As a further alternative, the counter may be arranged to be incremented by the number of bits in a data packet upon arrival of each data packet and to be decremented by Z upon transmission of each group of Z data bits, where Z is a positive integer.

The data packets may have sequence numbers and the counter may be arranged to be incremented upon arrival of a packet whose sequence number is greater than that of the previous packet to arrive at the buffer. The counter may be arranged to be incremented by the difference between the sequence numbers and to be decremented by one upon transmission of an amount of data equal to the content of a data packet. As an alternative, the counter may be arranged to be incremented by the product of the number of bytes in a data packet and the difference between the sequence numbers and to be decremented by Z upon transmission of each group of Z data bytes, where Z is a

positive integer. As a further alternative, the counter may be arranged to be incremented by the product of the number of bits in a data packet and the difference between the sequence numbers and to be decremented by Z upon transmission of each group of Z data bits, where Z is a positive integer.

Z may be equal to 1.

The apparatus may comprise an output arrangement for forming packets removed from the buffer into a time division multiplexed output stream.

According to a second aspect of the invention, there is provided a network interface comprising an apparatus according to the first aspect of the invention.

According to a third aspect of the invention, there is provided a method of regenerating a clock, comprising buffering data packets in a buffer, incrementing a count upon arrival of each data packet by a first amount representing the amount of data in the packet, decrementing the count by a second amount representing the amount of transmitted data, applying a filter function having a low pass component to the count, supplying the regenerated clock to control the timing of data transmission, and controlling the frequency of the regenerated clock in accordance with the filtered count.

The invention will be further described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block schematic diagram illustrating a leased line service and showing a network interface including an apparatus for regenerating a clock constituting an embodiment of the invention; and

Figure 2 is a block schematic diagram of the clock regenerating apparatus.

Figure 1 illustrates a time division multiplexed (TDM) circuit for providing a leased line service over a carrier network 1 comprising a packet switched network from a first

customer premises 2 to a second customer premises 3. The packet network 1 may, for example, be an Ethernet, ATM or IP. In the customer premises 2, customer data such as voice signals for a telephone connection are supplied to a transmitter 4 controlled by a clock generator 5. The transmitter 4 forms the data for transmission into TDM format with the rate of transmission of packets being substantially constant and being determined by the frequency $f_{service}$ of the clock generator 5.

The TDM flow is supplied to a first network interface 6, which converts the TDM signals into packets such as 7. Each packet carries a payload of data together with a destination address, for example in a packet header, indicating the address for delivery which, in this case, is a further network interface 8. The interface 8 comprises a packet delay variation buffer 9 containing a packet queue of those packets which have been received via the network but which have not yet been onwardly transmitted.

The interface 8 comprises an output arrangement 10, which takes packets from the queue in the buffer 9 in accordance with a regenerated clock signal of frequency f_{regen} supplied by a clock regenerating apparatus 11. The transmitter 10 forms the packets into an output TDM stream supplied to the customer premises 3. The premises 3 comprise a receiver 12 controlled by a clock generator 15, which extracts the clock frequency f_{regen} from the incoming data stream. The rate of transmission of packets from the customer premises 2 to the interface 6 of the network 1 is substantially constant and is determined by the frequency $f_{service}$. However, the rate of packet arrival at the interface 8 may be perturbed by the intervening packet network. For example, packets typically arrive at the interface 8 in bursts separated by varying amounts of delay. The delay between successive packets and bursts varies depending on the amount of traffic in the network 1. Although the characteristics of the network 1 are non-deterministic, the long term average rate of arrival of packets at the interface 8 is equal to the rate of departure of packets from the premises 2.

The clock regenerating apparatus 11 is required to supply a clock with a frequency f_{regen} which matches that $f_{service}$ of the clock generator 5. The buffer 9 has a size sufficient to cope with variations in packet arrivals from the packet network. The size of the packet

queue which forms in the buffer 9 is a compromise between being large enough to ensure that packets are available when required by the output arrangement 10 for most packet delays which may occur in the network and being small enough so as to reduce the latency of the communication link.

The clock regenerating apparatus is illustrated in more detail in Figure 2. The apparatus comprises the buffer 9 containing the packet queue 20 and the TDM output arrangement 10 shown in Figure 1, together with a packet input arrangement 21 for receiving packets from the network and storing them in the buffer 9. The clock regeneration apparatus comprises a digitally controlled oscillator 22, which supplies regenerated bit rate clock signals (and other clock signals derived therefrom, for example by frequency division) to the buffer 9 and the output arrangement 10. The oscillator 22 supplies the regenerated clock signal with a frequency determined by a clock control algorithm formed by a controller 23.

The apparatus also comprises a packet counter 24, which is incremented each time a packet is added to the queue 20 by the packet input arrangement 21 and decremented each time an amount of data corresponding to the content of a packet is removed from the queue 20 in accordance with a regenerated clock signals. For example, the bit rate clock signals may be divided in frequency by the number of bits in a packet and the resulting signal may be used to decrement the counter 24. The counter 24 thus provides a count which is representative of, but not necessarily equal to, the number of packets currently in the packet queue 20 within the buffer 9.

The count may differ from the number of packets in the queue 20 for various reasons. For example, the buffer content cannot fall below zero whereas the count in the packet counter 24 may do so. Also, where the buffer 9 is of limited size, and becomes full, the counter 24 can be incremented by packets which are thrown away and thus are not stored in the queue 20. Thus, the packet counter 24 has a larger bipolar range than the range of contents of the queue 20 and the count or the filtered count may be different from the number of packets actually in the queue 20 at any time. Such an arrangement

improves the performance of clock regeneration as compared, for example, with using the actual number of packets (possibly filtered) in the queue 20 for clock regeneration.

The count provided by the counter 24 is supplied to a digital filter 25, which supplies the filtered count to the controller 23. On the basis of the filtered count, the controller 23 adjusts the frequency of the oscillator 22 in such a way as to tend to reduce the difference between the actual count and an offset representing the desired number of packets in the packet queue 20.

When each packet arrives at the packet input arrangement 21, the count in the packet counter 24 is incremented by 1. Also, the packet is placed in the packet queue 20 in the buffer 9 if this is possible or desirable depending on the circumstances. For example, a packet may be discarded if the queue is of limited size and is already full. Alternatively, a packet may be classified as late or early and may be discarded.

The rate at which packets are received is determined by the source TDM clock frequency $f_{service}$ and variations in propagation delay across the network 1. The rate at which the queue 20 is emptied is determined by the frequency f_{regen} of the regenerated clock provided by the oscillator 22. The count in the packet counter 24 is decremented by 1 each time an amount of data equal to the data content of a packet is taken from the buffer 9 to be transmitted from the output arrangement 10. Thus, if the packet delay across the network were fixed, the packet count would increase if $f_{service}$ were greater than f_{regen}, would decrease if f_{regen} were greater than $f_{service}$, and would remain substantially constant if the frequencies were identical.

The filter 25 is shown as sampling the count in the counter 24 at intervals determined by the frequency of the oscillator 22. Alternatively, the filter 25 may sample the count at other intervals which may be related or unrelated to the frequency of the oscillator 22. For example, the actual sampling interval may be programmable.

Although the controller 23 may perform its control algorithm at intervals which may be determined by the frequency of the oscillator 22, this is not necessary. In general, the

control algorithm is performed at much longer intervals than used by the filter 25. For example, where the controller 23 is embodied as a central processing unit (CPU) separate from other parts of the apparatus, the intervals may be based on a CPU timer or on an interrupt supplied by the apparatus but not necessarily derived from the output of the oscillator 22.

The filter 25 performs a filtering function having a low pass component, such as a low pass filter, and supplies the filtered count to the controller 23. The controller 23 performs a calculation to determine a correction to the frequency of the oscillator 22 for causing the regenerated clock frequency f_{regen} to converge to the clock frequency $f_{service}$. By controlling the frequency of the oscillator 22 so as to maintain a substantially constant count in the packet counter 24, the regenerated clock frequency f_{regen} is phase-locked to the frequency $f_{service}$ and maintains a substantially constant number of packets in the queue 20.

The filtering performed by the filter 25 removes or reduces fluctuations in the count in the packet counter 24 so that fluctuations in the count because of the burst nature of the incoming packet stream do not cause unacceptably large fluctuations in the frequency f_{regen} of the regenerated clock. The filter 25 also performs an anti-aliasing function. The filter 25 may be embodied in hardware separate from that providing the controller 23 and may, for example, be embodied as hard-wired hardware, i.e. whose function is determined by circuit structure rather than programming but which may permit parameters of the function to be programmed. Separating the filtering function from the clock control algorithm allows the numerical processing workload in the clock control algorithm to be reduced. The controller 23 may be implemented by a central processing unit, which may be external to the other parts of the clock regenerating apparatus. Also, the workload of the clock control algorithm may be reduced by allowing the clock control interval to be increased.

In a specific embodiment, the filter 25 is a first order low pass filter comprising hardware implementing the following difference equation, which does not require any

dividers or multipliers (division by a power of 2 may be achieved simply by shifting bit positions):

$$Y_n = Y_{n-1} + (X_n - Y_{n-1}) / 2^P$$

Where Y_n is the filter output, X_n is the packet count, P is a programmable parameter which determines the time constant of the filter, and $_n$ is the sample number which increments each time a packet is removed from the packet queue 20.

The clock control algorithm reads the filter output Y_n, determines the required correction, and writes the required frequency to the digitally controlled oscillator 22. A suitable control algorithm for performing phase-locking is given by the following difference equation:

$$F_m = F_{m-1} + G1\ (Y_m - Y_{m-1}) + G2\ (Y_m - Offset)$$

Where F_m is the frequency to be written to the oscillator 22, G1 and G2 are constants (which may be programmable) for determining the dynamic behaviour of the control algorithm, F_{m-1} is the current frequency of the oscillator 22, Y_m is the filter output, "Offset" is a constant to determine the average size of the packet queue, and $_m$ is the sample number which increments each time the clock control algorithm reads the filter output. The parameters G1 and G2 determine the frequency response and transient response of the control loop and are generally selected to track long term drift in the frequency $f_{service}$ but to reject short term variations due to packet delay variations across the network 1. Effectively, the G1 term provides frequency locking whereas the G2 term provides phase locking by introducing a deviation for driving the packet count to the desired "Offset".

"Offset" may be used to build the average operating packet queue depth in the following way. Initially, the queue is empty and the counter 24 is set to zero. When packets start to arrive, for instance by enabling the packet input arrangement 21, the clock control algorithm builds the average number of packets maintained in the queue 20 to the

"Offset" value and stabilises this value. Similarly, "Offset" may be adjustable or programmable and may, for example, be used during operation to adjust the average queue depth to a new value, for example if network conditions change.

In one embodiment of such an arrangement, the actual content of the queue 20, or a filtered version of this, may be compared with the filtered count and any difference may be used to adjust the value of "Offset" so as to stabilise the required buffer depth.

As an alternative, some other technique may be used to establish the packet queue depth and the count in the counter 24 may be initialised to the "Offset" value.

The filter and clock control algorithms disclosed hereinbefore are given as examples and other algorithms may be used. For example, alternatives to the clock control algorithm include higher order algorithms, fuzzy logic, neural networks and self-tuning algorithms which vary their parameters over time.

In an alternative arrangement, the packet counter 24 may count bits or bytes instead of packets. For example, when a packet arrives, the counter 24 may be incremented by the number of payload bits or bytes in the packet. The counter may then be decremented by 1 whenever the output of the oscillator 22 indicates that a bit or byte has been transmitted by the TDM output arrangement 10, or may be decremented by a positive integer Z greater than one when a group of Z bits or bytes has been transmitted by the arrangement 10.

Where the packets contain sequence numbers, the counter 24 may be incremented in a way which takes into account packets which have been lost in transit across the network 1. Such an arrangement improves the performance of clock recovery for networks in which a significant percentage of packets is lost. In this case, when a packet arrives, its sequence number is compared with that of the previous packet to arrive. If the latest packet has a higher sequence number than the previous packet, then the counter 24 is incremented by the difference between the sequence numbers or by that difference multiplied by the number of bytes or bits per packet. Otherwise, the counter 24 is not

incremented. In this case, where the sequence numbers of packets "wraparound", this must be taken into account when incrementing the counter 24. The counter 24 is then decremented as described above.

It is thus possible to provide an efficient and elegant technique for regenerating a clock, for example for TDM or other synchronous applications, when such synchronous links are emulated across an asynchronous network, such as a packet switching network. No special timing packets or timing information are required and expensive clock generation circuits, such as oven-controlled crystal oscillators, are not required. It is possible to use a high speed filter 25 which is separate from a lower speed clock control algorithm and such an arrangement has significant benefits, such as flexibility, reduction of development time, and ease of optimisation for a specific environment.

CLAIMS:

1. An apparatus for regenerating a clock, comprising a buffer for buffering data packets, a counter arranged to be incremented upon arrival of each data packet by a first amount representing the amount of data in the packet and to be decremented by a second amount representing the amount of data transmitted from the apparatus, a digital filter for performing a filter function having a low pass component on the count in the counter, a digitally controlled oscillator for supplying the regenerated clock to control the timing of data transmission, and a controller for controlling the frequency of the oscillator in accordance with the filtered count.

2. An apparatus as claimed in claim 1, in which the controller is arranged to control the frequency of the oscillator so as to reduce the difference between the amount of packet data in the buffer and a predetermined amount.

3. An apparatus as claimed in claim 1 or 2, in which the filter and the controller are embodied as separate hardware.

4. An apparatus as claimed in claim 3, in which the filter is embodied as hard-wired hardware.

5. An apparatus as claimed in any one of the proceeding claims, in which the filter comprises a first order low pass filter.

6. An apparatus as claimed in claim 5, in which the filter is arranged to form a series of samples, Y_n, each of which is given by:

$$Y_n = Y_{n-1} + (X_n - Y_{n-1}) / 2^P$$

where $_n$ is the sample number, X_n is the count, and P is a parameter.

7. An apparatus as claimed in claim 6, in which P is programmable.

8. An apparatus as claimed in claim 6 or 7, in which the controller is arranged to form a series of samples F_m representing the frequency of the oscillator and given by:

$$F_m = F_{m-1} + G1\ (Y_m - Y_{m-1}) + G2\ (Y_m - Offset)$$

where $_m$ is the sample number and G1 and G2 are parameters.

9. An apparatus as claimed in claim 8, in which at least one of G1 and G2 is programmable.

10. An apparatus as claimed in any one of the preceding claims, in which the counter is arranged to be incremented by 1 upon arrival of each data packet and to be decremented by 1 upon transmission of an amount of data equal to the content of a data packet.

11. An apparatus as claimed in any one of claims 1 to 9, in which the counter is arranged to be incremented by the number of bytes in a data packet upon arrival of each data packet and to be decremented by Z upon transmission of each group of Z data bytes, where Z is a positive integer.

12. An apparatus as claimed in any one of claims 1 to 9, in which the counter is arranged to be incremented by the number of bits in a data packet upon arrival of each data packet and to be decremented by Z upon transmission of each group of Z data bits, when Z is a positive integer.

13. An apparatus as claimed in any one of claims 1 to 9, in which the data packets have sequence numbers and the counter is arranged to be incremented upon arrival of a packet whose sequence number is greater than that of the previous packet to arrive at the buffer.

14. An apparatus as claimed in claim 13, in which the counter is arranged to be incremented by the difference between the sequence numbers and to be decremented by 1 upon transmission of an amount of data equal to the content of a data packet.

15. An apparatus as claimed in claim 13, in which the counter is arranged to be incremented by the product of the number of bytes in a data packet and the difference between the sequence numbers and to be decremented by Z upon transmission of each group of Z data bytes, where Z is a positive integer.

16. An apparatus as claimed in claim 13, in which the counter is arranged to be incremented by the product of the number of bits in a data packet and the difference between the sequence numbers and to be decremented by Z upon transmission of each group of Z data bits, where Z is a positive integer.

17. An arrangement as claimed in any one of claims 11, 12, 15 and 16, in which Z is equal to one.

18. An apparatus as claimed in any one of the preceding claims, comprising an output arrangement for forming packets removed from the buffer into a time division multiplexed output stream.

19. A network interface comprising an apparatus as claimed in any one of the preceding claims.

20. A method of regenerating a clock, comprising buffering data packets in a buffer, incrementing a count upon arrival of each data packet by a first amount representing the amount of data in the packet, decrementing the count by a second amount representing the amount of transmitted data, applying a filter function having a low pass component to the count, supplying the regenerated clock to control the timing of data transmission, and controlling the frequency of the regenerated clock in accordance with the filtered count.

ABSTRACT

APPARATUS FOR AND METHOD OF REGENERATING A CLOCK AND NETWORK INTERFACE

An apparatus is provided for regenerating a clock, for example for emulation of TDM circuits across packet networks. The apparatus comprises a buffer 9 for buffering data packets and a counter 24 for containing a count representing the amount of packet data in the buffer 9. A digital filter 25 performs a filter function having a low pass component on the count in the counter 24. A digitally controlled oscillator 22 supplies the regenerated clock to control the timing of packet removal from the buffer 9. A controller 23 controls the frequency of the oscillator in accordance with the filtered output so as to control the oscillator frequency to reduce the difference between the amount of packet data in the buffer 9 and a predetermined amount.

(Figure 2)

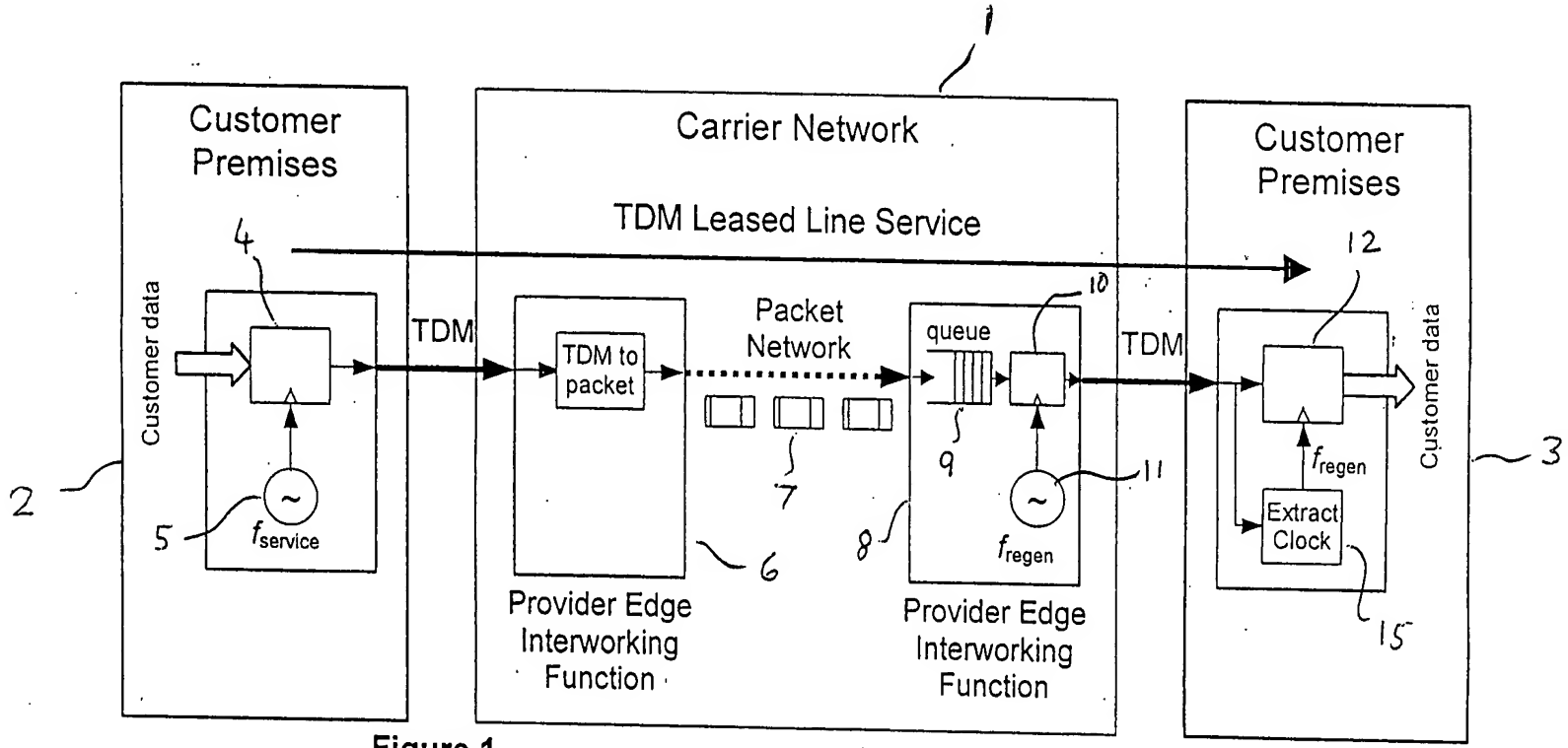
1
Customer Premises
Carrier Network
TDM Leased Line Service
Customer Premises
4
12
Customer data
TDM
TDM to packet
Packet Network
queue
10
TDM
Customer data
2
5
$f_{service}$
7
9
11
f_{regen}
3
8
6
f_{regen}
Extract Clock
15
Provider Edge Interworking Function
Provider Edge Interworking Function

Figure 1

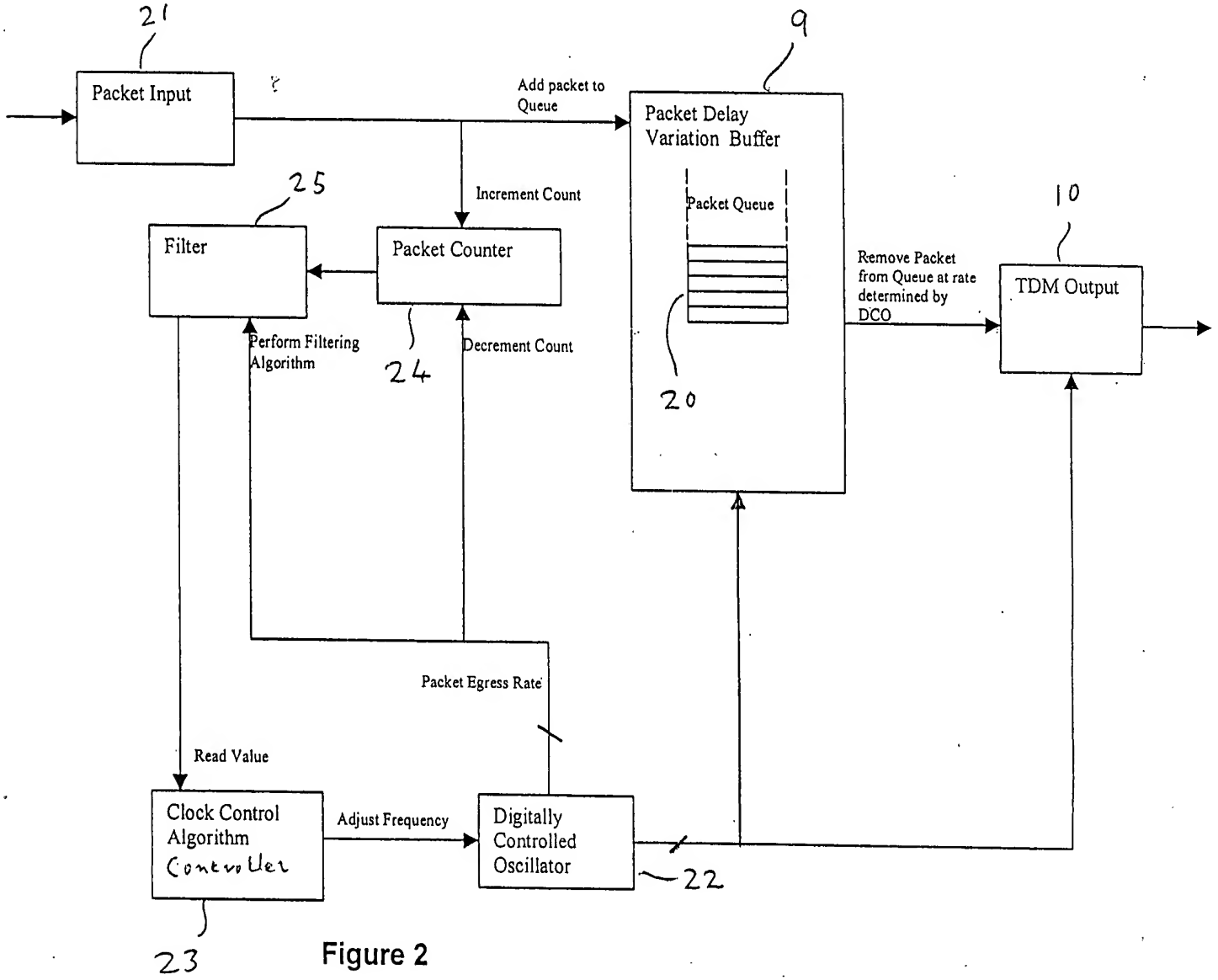
21
Packet Input
Add packet to Queue
9
Packet Delay Variation Buffer
Packet Queue
20
25
Filter
Increment Count
Packet Counter
24
Perform Filtering Algorithm
Decrement Count
Remove Packet from Queue at rate determined by DCO
10
TDM Output
Packet Egress Rate
Read Value
Clock Control Algorithm
Controller
Adjust Frequency
Digitally Controlled Oscillator
22
23

Figure 2